

C65C02

65C02-compatible Microprocessor

MAJOR FEATURES

- ◆ 65C02 ISA compliant
- ◆ Control Unit with both maskable and non-maskable interrupts
- ◆ 8-bit Instruction Decoder with 69 instructions and 212 documented opcodes
- ◆ 8-bit ALU for decimal and binary arithmetic as well as logical/ logical shift operations
- ◆ External Memory interface addressing up to 64KB of memory through 16 addressing modes
- ◆ Power saving mode

OVERVIEW

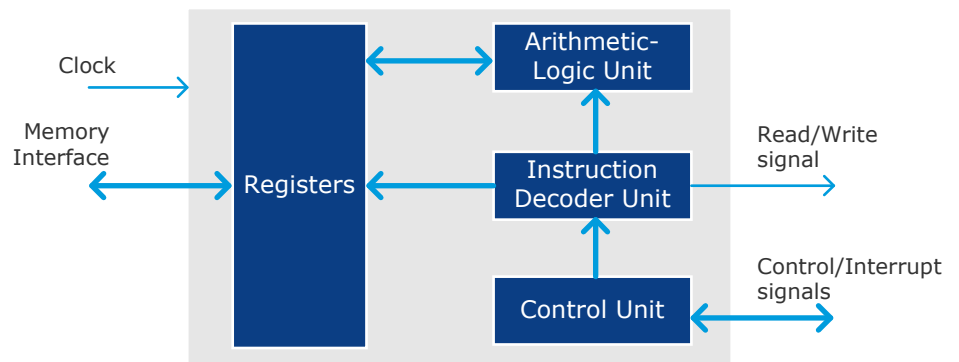
The **C6502** is a fast 8-bit microprocessor IP core that implements the same instruction set as the 65C02 microprocessor, which is an upgraded version of the popular NMOS-based MOS Technology 6502 8-bit CPU. The **C65C02** provides software and hardware interrupts for interfacing external devices.

With sixteen addressing modes, including indirect index and zero page, the **C6502** is able to address up to 64KB of external memory with two byte long instructions.

The 8-bit arithmetic-logic unit can operate on signed and unsigned binary numbers as well as binary-coded decimal numbers.

The C65C02 core offers two instructions for efficient power management: STP for halt processor and WAI for wait for interrupt instruction.

BLOCK DIAGRAM



C65C02

BENEFITS

- ◆ 65C02 architecture popularity results in a large variety of industry-certified software ready to be used with the core
- ◆ Obsolete IP cores, on contrary to original chips, can be easily integrated in more advanced SoC designs targeted to FPGAs or ASICs
- ◆ Having the IP core of the processor guarantees independence from the chip vendor
- ◆ Possibility to modify the instruction list according to customer's application

APPLICATIONS

- ◆ 8-bit data processing applications
- ◆ Low power consumption applications
- ◆ High speed control systems
- ◆ Microcomputer systems

STANDARD DELIVERABLES

- ◆ VHDL/Verilog source code
- ◆ Synthesis support for Synopsys® tools with a set of synthesis scripts
- ◆ Simulation support for Mentor Graphics® and Cadence® tools with a set of scripts and macros
- ◆ Extensive VHDL/Verilog 2001 test bench
- ◆ Documentation:
 - ▶ Design Specification
 - ▶ Verification Specification
 - ▶ Test Plan
 - ▶ Integration Manual
 - ▶ User Guide
- ◆ A collection of 65C02 assembler programs which are executed directly by the test bench
- ◆ 30 days of technical support
- ◆ 90 days of warranty against defects

DELIVERY OPTIONS

- ◆ EDIF netlist for FPGA and low volume production
- ◆ Evaluation system for proprietary **EB5-Tiny** board
- ◆ One-year maintenance
- ◆ On-site support and training



For more information on our IP portfolio visit www.evatronix-ip.com



ELECTRONIC DESIGN DEPARTMENT

Dubois 16, 44-100 Gliwice, Poland
T: +48 32 231 11 71
F: +48 32 231 30 27

info@evatronix-ip.com
www.evatronix-ip.com