

MAJOR FEATURES

- ◆ Compliant with UTMI+ (level 3) specification,
- ◆ Support for Hi-Speed, Full and Low Speed data rates
- ◆ Built-in Self Test
- ◆ 8-bit and optional 16-bit parallel UTMI interface
- ◆ Internal self calibrated termination resistors
- ◆ Built in pull down and pull-up resistors
- ◆ 3.3V±10% analog supply and 1.8V±10% digital core supply
- ◆ IP includes decoupling cells for better performance
- ◆ Scan-based DFT and loop back

STANDARD DELIVERABLES

- ◆ Design files kit
- ◆ Extensive documentation
- ◆ 30 days of technical support
- ◆ 90 days of warranty against defects

RELATED PRODUCTS

USBHS-DEV - USB 2.0 High Speed device controller with UTMI/ULPI PHY interfaces and Generic/AMBA®/PVICI interfaces for the CPU.

USBFS-DEV - USB 2.0 Full Speed device controller with UTMI/ULPI PHY interfaces and generic/ AMBA®/PVICI interfaces for the CPU.

USBHS-PHY

USB 2.0 High, Full and Low Speed PHY for 45-180 nm processes

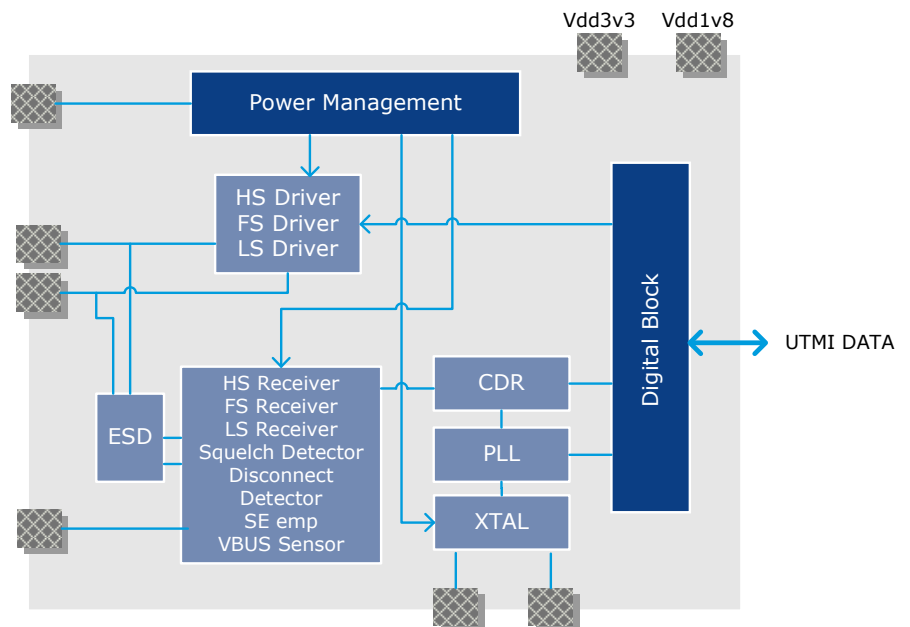
OVERVIEW

The USBHS-PHY is a complete mixed-signal transceiver macro-cell that implements the USB 2.0 Physical Layer for Host and Device applications.

TARGET TECHNOLOGY

The **USBHS-PHY** is currently available on the LFoundry 150nm process with the possibility to port it to any technology node from 45 to 180nm.

BLOCK DIAGRAM



For more information on our IP portfolio visit www.evatronix.com/ip