

# USBSS-DEV

USB-IF Certified SuperSpeed USB 3.0 Device Controller



## MAJOR FEATURES

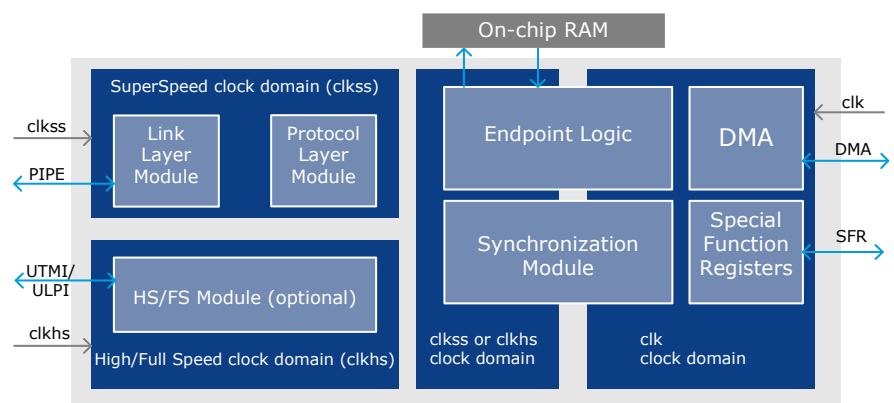
- ◆ Certified for compliance with the latest revision of the USB 3.0 specification
- ◆ High/Full Speed support with the UTMI interface (optional)
- ◆ Configurable 8/16/32/64-bit OCP Slave/AMBA® AHB interfaces
- ◆ DMA controller with a configurable 32/64-bit OCP Master/AMBA® AHB interface
- ◆ Configurable USB 3.0 PIPE interface (8/16/32/64-bit)
- ◆ Optional PLB or OPB bus interface wrappers
- ◆ Control transfers supported by Endpoint 0
- ◆ Up to 15 IN and 15 OUT configurable/programmable endpoints
- ◆ Synchronous Single Port RAM interface for endpoint buffers
- ◆ Full Power Management capabilities (U1, U2 & U3 ) with LFPS support
- ◆ Supports bulk, interrupt and isochronous transfers
- ◆ Bulk Stream support

## OVERVIEW

The **USBSS-DEV** IP core logic provides SuperSpeed USB (5 Gbps) function interface that is certified by the USB Implementers Forum to be compatible with the latest revision of the USB 3.0 specification.

The **USBSS-DEV** logic handles bytes transfer autonomously and bridges USB interface to the OCP or AMBA® AHB interface or, upon request, to OPB or PLB bus interfaces. The **USBSS-DEV** can be customized and optimized for a specific application.

## BLOCK DIAGRAM



# USBSS-DEV

## BENEFITS

- ◆ USB-IF certified solution
- ◆ Complete hardware and software solution
- ◆ High level of configurability
- ◆ Industry standard interfaces that simplify system integration
- ◆ Verilog coding style for true technology independence
- ◆ Customization to fit user needs
- ◆ Flexible licensing schemes

## APPLICATIONS

- ◆ Mass storage applications
- ◆ Audio/video applications
- ◆ Communication devices
- ◆ Digital cameras
- ◆ Networking
- ◆ Digital Media Controllers

## CONFIGURABILITY

- ◆ Data bus width of the USB 3.0 PIPE interface
- ◆ Optional USB 2.0 High Speed/Full Speed support
- ◆ Configurable ULPI or UTMI interface
- ◆ Data bus width of the OCP Master/ and Slave and AMBA® AHB interfaces
- ◆ Number of endpoints
- ◆ Size of the On-Chip buffers

## STANDARD DELIVERABLES

- ◆ Verilog source code
- ◆ A choice of OCP or AMBA® AHB system bus interface
- ◆ Extensive SystemC Test Bench with a TLM model of the **USBSS-DEV**
- ◆ Synthesis support with a complete set of synthesis scripts
- ◆ Simulation support with a set of scripts and macros
- ◆ A collection of tests which are executed directly by the Test Bench
- ◆ Additional documentation:
  - Design Specification
  - Verification Specification
  - Test Plan
- ◆ Design support including consulting
- ◆ 30 days of technical support
- ◆ 90 days of warranty against defects

## DELIVERY OPTIONS

- ◆ OPB or PLB bus interface wrappers
- ◆ EDIF netlist for FPGA and low volume production
- ◆ One-year maintenance
- ◆ On-site support
- ◆ On-demand modifications

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