

# SPDIF

Sony®/Philips® Digital Interface Controller

## MAJOR FEATURES

- ◆ Meets the SPDIF specification
- ◆ AMBA® AHB/APB, OPB, PLB and Avalon system bus interfaces available
- ◆ Receiver/Transmitter modes are supported
- ◆ Support for sample rates from 3kHz to 192 kHz (with 98MHz SPDIF system clock), 20/24 bit per sample
- ◆ Integrated AMBA® APB or AMBA® AHB slave wrapper to interface with the host AHB or APB controller
- ◆ DMA Master handshake interfacing
- ◆ Configurable size of external FIFO (default value is 64 words)
- ◆ Power safe capability
- ◆ Internal, event stimulated, interrupt request generation with masking capability
- ◆ Synchronization hold in the under run condition
- ◆ Clock recovery from the SPDIF data stream
- ◆ Detection of sample rate from the received data stream
- ◆ Variable baud rate

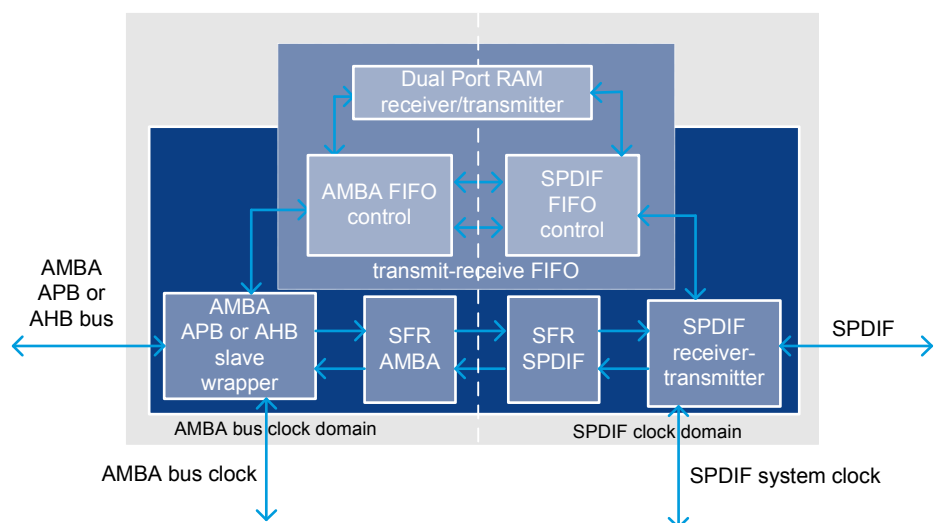
## OVERVIEW

The **SPDIF** controller implements the IEC 60958 interface features (commonly known as Sony®/Philips® Digital Interface), a unidirectional and self-clocking interface for connecting digital audio equipment using the linear PCM coded audio samples.

All data collected by the **SPDIF** controller are stored in the internal core's FIFO memory. The use of internal FIFO allows the system to process relatively slow audio stream in the interrupt triggered subroutines.

The **SPDIF** can be also easily used for fast serial non-audio transmission. The **SPDIF** controller core can be easily integrated with the master system based on standard AMBA® APB or AMBA® AHB bus interface for further data processing.

## BLOCK DIAGRAM



# SPDIF

## BENEFITS

- ◆ Advanced configurability
- ◆ Full resistance to input signal jitter defined by the IEC 60958
- ◆ Configurable internal FIFO for data streaming
- ◆ Compact, high performance architecture

## APPLICATIONS

- ◆ Digital audio, video (DVD) and multimedia systems in general
- ◆ High quality multi channel audio transmission – non PCM data
- ◆ Fast serial non-audio transmission
- ◆ Applications where optical serial communication is required (high immunity for EMC, low vulnerability for electrostatic discharge, secure systems with reduced EMC radiation)

## STANDARD DELIVERABLES

- ◆ VHDL/Verilog source code
- ◆ Synthesis support for Synopsys® and Cadence® tools with a set of synthesis scripts
- ◆ Simulation support for Mentor Graphics® and Cadence® tools with a set of scripts and macros
- ◆ Extensive VHDL/Verilog 2001 test bench
- ◆ Documentation:
  - ▶ Design Specification
  - ▶ Verification Specification
  - ▶ Test Plan
  - ▶ Integration Manual
- ◆ 30 days of technical support
- ◆ 90 days of warranty against defects

## DELIVERY OPTIONS

- ◆ EDIF netlist for FPGA and low volume production
- ◆ One-year maintenance
- ◆ On-site support and training



For more information on our IP portfolio visit [www.evatronix-ip.com](http://www.evatronix-ip.com)



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