

SDLC

Synchronous Data Link Control Protocol Controller

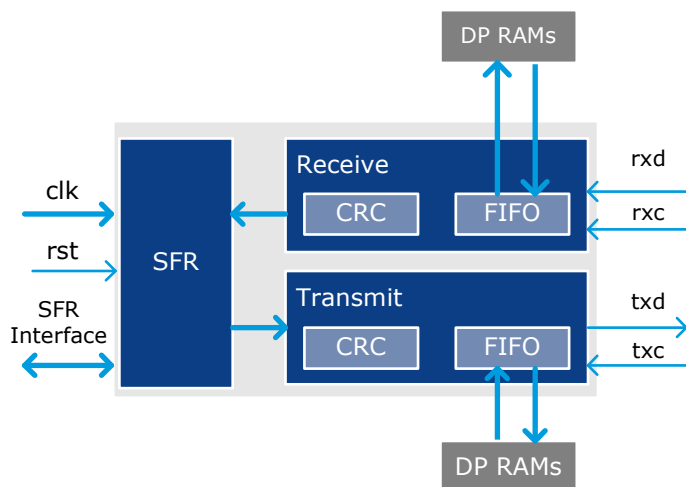
MAJOR FEATURES

- ◆ Based on 8XC152 Global Serial Channel
- ◆ AMBA® APB or generic system bus interface
- ◆ Configurable size of transmit and receive FIFOs
- ◆ Single and double byte address recognition
- ◆ 16/32-bit frame check sequence
- ◆ NRZ and NRZI data encoding
- ◆ Automatic bit stuffing/stripping
- ◆ Full or half duplex operation
- ◆ Variable baud rate
- ◆ External or internally generated transmit/receive clocks

OVERVIEW

The **SDLC** controller provides a high speed synchronous serial communication interface. Operation of the controller is similar to that used in Intel® 8XC152 Global Serial Channel (GSC) working in SDLC mode under CPU control. Communication with CPU is realized through Special Function Registers (SFRs) and 3 interrupt sources. This allows the **SDLC** controller for an easy integration into any CPU core.

BLOCK DIAGRAM



SDLC

BENEFITS

- ◆ Simple in use, low area design
- ◆ Optimized to support low cost and low power requirements of medium and low traffic systems
- ◆ Can be used as a general purpose synchronous interface with only single line (clock recovered from a data stream)
- ◆ Easy integration with SoC systems through a generic 8-bit interface

APPLICATIONS

- ◆ ISDN D-channel
- ◆ X.25 networks
- ◆ Frame Relay networks
- ◆ Custom serial interfaces

STANDARD DELIVERABLES

- ◆ VHDL/Verilog source code
- ◆ Synthesis support for Synopsys® tools with a set of synthesis scripts
- ◆ Simulation support for Mentor Graphics®, Aldec® and Cadence® tools with a set of scripts and macros
- ◆ Extensive test bench
- ◆ Documentation:
 - › Design Specification
 - › Verification Specification
 - › Integration Manual
- ◆ 30 days of technical support
- ◆ 90 days of warranty against defects

DELIVERY OPTIONS

- ◆ EDIF netlist for FPGA and low volume production
- ◆ One-year maintenance
- ◆ On-site support and training



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