

# ATAIF

## Parallel ATA Disk Host Controller

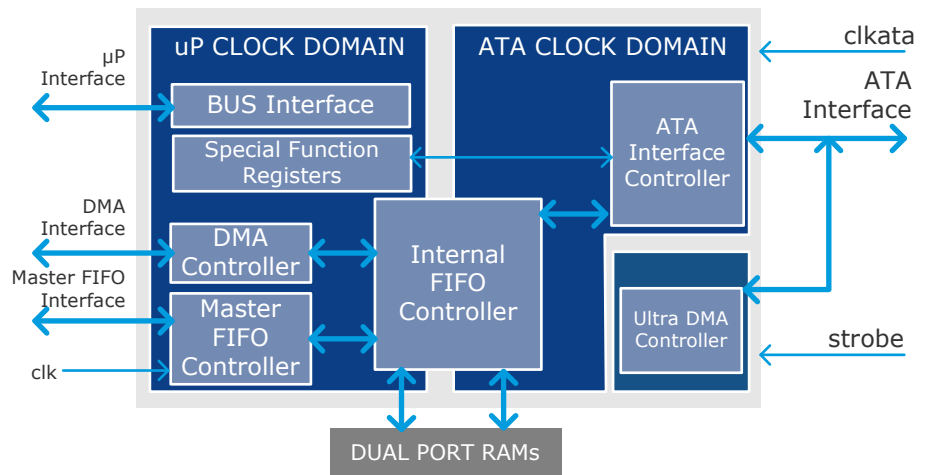
### MAJOR FEATURES

- ◆ Supports one or two IDE devices
- ◆ Supports synchronous Ultra ATA-33, -66, -100 and -133
- ◆ Programmable I/O modes: 0, 1, 2 and 4
- ◆ Multi-word DMA modes: 0, 1 and 2
- ◆ Generic SFR interface with a configurable 8/16/32-bit data bus
- ◆ Configurable internal FIFO address bus width - min. 4-bit, no upper limit
- ◆ Uses either the DMA Controller or the Master FIFO controller for the data transmission interface
- ◆ DMA controller delivers configurable data and address buses and works in both master and slave modes
- ◆ Master FIFO interface has a direct connection to Evatronix USBHS-DEV and USBHS-OTG controllers
- ◆ Transmit/Receive buffers operate as internal configurable FIFOs

### OVERVIEW

The **ATAIF** implements a host controller for non-volatile memory devices using the parallel interface known as ATA (Advanced Technology Attachment), IDE (Integrated Drive Electronics), and ATAPI (Advanced Technology Attachment Packet Interface). The IP provides a simple interface to memory devices such as hard-disk drives, CDROM/DVD players/writers, Compact Flash storage, and PC Card devices. It supports PIO modes 0 to 4; Multi-word DMA modes 0, 1 and 2; Ultra ATA -33, -66, -100 and -133; and implements an interface to the IDE bus.

### BLOCK DIAGRAM



# ATAIF

## BENEFITS

- ◆ Complies with ATA-8 Standard
- ◆ Flexible, can be configured for connectivity and control of various mobile, peripheral and memory technologies
- ◆ The optional ATAIF Software Driver provides the user with a full access to the functionality provided by the ATAIF host controller core

## CONFIGURABILITY

The following parameters allow adjusting the **ATAIF** core to requirements of target application or technology:

- ◆ SFR data bus width
- ◆ DMA address/data bus width
- ◆ Master FIFO data bus width
- ◆ Configurable Internal FIFO address bus width
- ◆ Size of the counter for transmission size

The DMA controller block can be implemented alternatively instead of Master FIFO controller.

## APPLICATIONS

- ◆ IDE disk drive, CDROM player/writer & DVD player controllers
- ◆ Compact Flash and PC-Card readers
- ◆ Systems utilizing IDE/ATA and ATAPI drives for data storage including notebook and desktop computers, servers, set-top boxes and test equipment
- ◆ Data acquisition systems

## RELATED PRODUCTS

**ATAIF\_SD** - a complete software set for handling the **ATAIF** host controller. It supplements **ATAIF** controller with software elements and enables a smooth integration of the controller in a target application, allowing user to easily access storage media of high capacity without detailed knowledge of the controller interface.

**ATAIF\_SD-LNX** - a complete software set allowing higher-level Linux kernel to interact with the Evatronix ATAIF IP core.

## STANDARD DELIVERABLES

- ◆ VHDL/Verilog source code
- ◆ Synthesis support for Synopsys® and Cadence tools with a set of synthesis scripts
- ◆ Simulation support for Mentor Graphics® and Cadence® tools with a set of scripts and macros
- ◆ Extensive VHDL/Verilog 2001 test bench
- ◆ Documentation:
  - ▶ Design Specification
  - ▶ Verification Specification
  - ▶ Test Plan
  - ▶ Integration Manual
  - ▶ User Guide
- ◆ 30 days of technical support
- ◆ 90 days of warranty against defects

## DELIVERY OPTIONS

- ◆ EDIF netlist for FPGA and low volume production
- ◆ Reference design for proprietary evaluation board
- ◆ AMBA® AHB, OPB or Avalon system bus interface
- ◆ One-year maintenance
- ◆ On-site support and training



For more information on our IP portfolio visit [www.evatronix-ip.com](http://www.evatronix-ip.com)



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