

NANDFLASH-CTRL

NAND Flash Memory Controller

MAJOR FEATURES

- ◆ Support for High Speed NAND Flash memories (up to 200 MB/s)
- ◆ Support for Toggle Mode DDR NAND Flash devices
- ◆ Support for Standard and Enhanced ClearNAND
- ◆ Compatible with ONFi 1.x and 2.2 standards as well as ONFi standard following manufacturers (Micron®)
- ◆ Support for all popular standard memory device manufacturers (Samsung®, Toshiba®)
- ◆ Up to 64-bit BCH Error Correction Code (ECC) calculation and data correction
- ◆ The controller allows both SLC and MLC to be connected simultaneously
- ◆ Super Sequence - Multipage transfer – support for transferring sequence of data blocks - reducing software overhead
- ◆ Encryption Support - AES-256 option engine embedded in data path
- ◆ OCP socket for straightforward implementation into custom system bus interfaces
- ◆ Available with AMBA® AHB, PLB, Avalon and FlexBus system bus interfaces
- ◆ Automatic Write/Read Page with data correction

OVERVIEW

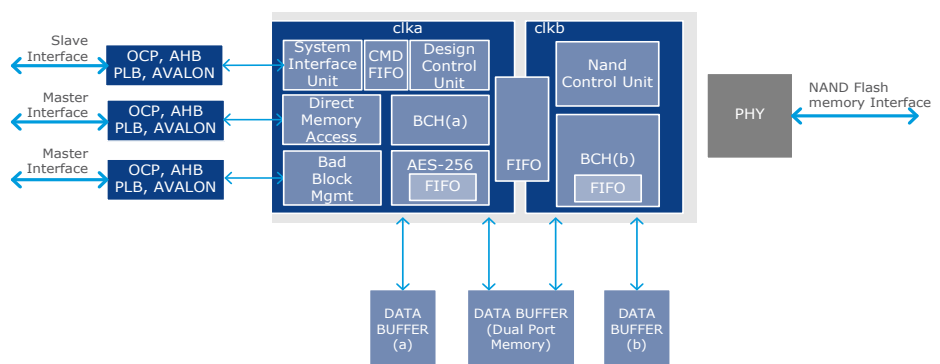
This ONFi 2.2 compliant **NANDFLASH-CTRL** IP core for high-capacity Multi-Level Cell (MLC), Single-Level Cell (SLC) and High-Speed NAND Flash memories provides System-on-Chip developers with a comprehensive way to minimize time-consuming hardware and software development as well as leverage emerging embedded application technologies.

In the latest release, there has been added support for Clear NAND memories from Micron and Toggle Mode DDR devices from Samsung and Toshiba.

For more efficient application development, the IP core is designed to work seamlessly with the NANDFLASH-CTRL Software Driver, which relieves the higher level application layer from hardware management.

Implementation of High Speed NAND Flash memories compliant with ONFi 2.x can be facilitated with the implementation of a dedicated Synthesizable Digital Locked Loop PHY (**SDLL-NANDFLASH-PHY**) for the NAND Flash Memory Controller.

BLOCK DIAGRAM



NANDFLASH-CTRL

BENEFITS

- ◆ Support for ONFi 1.x and 2.2 standards speeds time-to-market
- ◆ Ability to connect SLC and MLC memories simultaneously
- ◆ Source synchronous (High Speed DDR mode) and asynchronous interfaces support
- ◆ Seamless SoC integration with a built-in OCP socket
- ◆ The BCH ECC algorithm allows up to 64-bit error correction
- ◆ IP configuration script for cutting obsolete functional blocks

APPLICATIONS

- ◆ Mass Storage - USB flash drives, digital cameras, digital voice recorders, Solid State Drives (SSD)
- ◆ Embedded Storage — cellular phones, network routers, point of sale systems

CONFIGURABILITY

- ◆ Big or Little Endian Type
- ◆ Number of banks and devices per bank
- ◆ Both source synchronous (DDR mode) and asynchronous or only asynchronous interfaces
- ◆ Support for 256 B to 16 kB page size
- ◆ Implementation of a DMA controller, Write/Erase Protection and hardware support for Bad Block Management
- ◆ BCH Error Correction Code
- ◆ Timing parameters
- ◆ Number of address cycles
- ◆ ECC calculation
- ◆ BCH strength
- ◆ Protected area size
- ◆ Implementation of interrupts

RELATED PRODUCTS

NANDFLASH-CTRL_SD - a low-level software driver that represents the first abstraction layer of the **NANDFLASH-CTRL** to relieve the higher level application layer from the hardware management.

SDLL-NANDFLASH-PHY - a Synthesizable Digital Locked Loop PHY for the NAND Flash Memory Controller that facilitates implementation of High-Speed NAND Flash memories compliant with ONFI 2.x.

STANDARD DELIVERABLES

- ◆ VHDL/Verilog source code
- ◆ Synthesis support for Synopsys® and Cadence tools with a set of synthesis scripts
- ◆ Simulation support for Mentor Graphics® and Cadence® tools with a set of scripts and macros
- ◆ Extensive Verilog test bench
- ◆ Documentation:
 - ▶ Design Specification
 - ▶ Verification Specification
 - ▶ Test Plan
 - ▶ Integration Manual
 - ▶ User Guide
- ◆ 30 days of technical support
- ◆ 90 days of warranty against defects

DELIVERY OPTIONS

- ◆ EDIF netlist for FPGA and low volume production
- ◆ One-year maintenance
- ◆ On-site support and training

We are a proud partner of



For more information on our IP portfolio visit www.evatronix.com/ip



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