

# I2S-SC

Philips® Inter-IC Sound Bus Single Channel Controller

## MAJOR FEATURES

- ◆ Meets Philips® Inter-IC Sound Bus specification
- ◆ I2S Philips, left/right justified, DSP channel and Time Division Multiplexing modes supported
- ◆ Native OCP socket with wrappers for AMBA® AHB, AMBA® APB or PLB system bus interfaces
- ◆ Support for one stereo channel with up to 16 optional channels (with TDM support)
- ◆ Two clock domains - host side and system clock
- ◆ One set of SCK (SCLK) and WS (LRCLK) strobes
- ◆ Separate, configurable FIFO buffer for transmit and receive channels
- ◆ Interrupts driven by the I<sup>2</sup>S bus activity events
- ◆ Handshake interface to external DMA modules

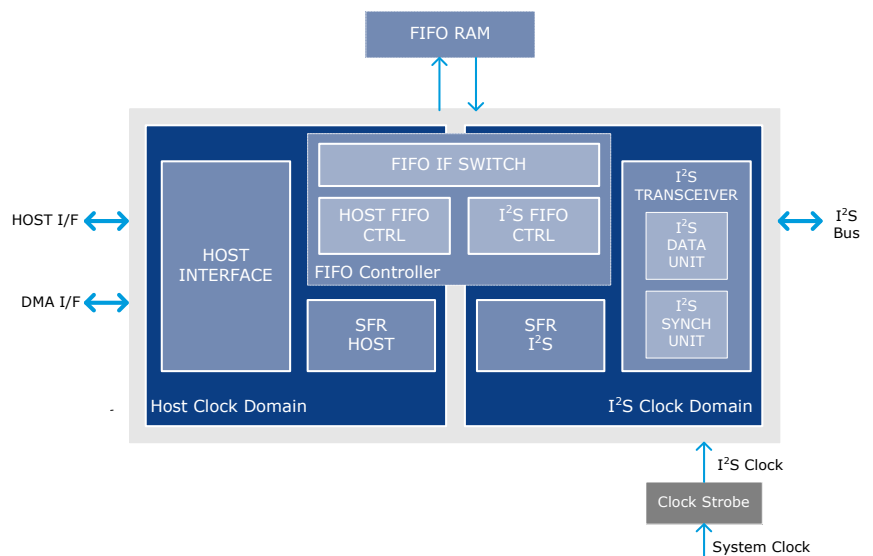
## OVERVIEW

The **I2S-SC** core is a configurable single channel Inter-IC Sound (I2S) bus interface controller that combines functions of both transmitter and receiver.

In order to facilitate the use of the **I2S-SC** core in various standard bus based microprocessor systems, different bus wrappers are provided, such as AMBA® AHB and APB, and CoreConnect™ PLB.

The **I2S-SC** core supports a wide range of transmission parameters that are configurable through SFR registers, thus extending the functionality of the core beyond the I<sup>2</sup>S standard.

## BLOCK DIAGRAM



# I2S-SC

## BENEFITS

- ◆ Simple development of I<sup>2</sup>S based digital audio interface with wide range of vendor specific transmission formats
- ◆ Flexible system bus type selection
- ◆ Single solution for standard I<sup>2</sup>S interface as well as for multichannel TDM interface

## CONFIGURABILITY

- ◆ Serial clock (SCK) polarity
- ◆ Word select (WS) polarity
- ◆ Frame synchronization / word select mode
- ◆ Audio channel width
- ◆ Data delay
- ◆ Data align within audio channel and host data bus
- ◆ Sample bit order
- ◆ Audio/mono mode
- ◆ Time Division Multiplexing (TDM) implementation
- ◆ Size of external FIFO (default value is 16 words)
- ◆ Width of data registers – maximum audio data width
- ◆ Host-side interface type
- ◆ Width of host data buses
- ◆ Size of external FIFO (default value is 16 words)

## PRODUCT VERSIONS

**I2S-MC** – Philips® Inter-IC Sound Bus controller that implements eight channels of Inter-IC Sound (I2S) serial buses and combines transmitter and receiver tasks.

## APPLICATIONS

- ◆ Applications requiring multiple channel audio data transmission
- ◆ Connecting Analog to Digital and Digital to Analog converters with very low jitter
- ◆ Digital audio interface of embedded microcontroller systems
- ◆ Error correction for compact disc and digital recording
- ◆ Digital signal processing and multimedia systems in general

## STANDARD DELIVERABLES

- ◆ VHDL/Verilog source code
- ◆ Synthesis support for Synopsys® and Cadence® tools with a set of synthesis scripts
- ◆ Simulation support for Mentor Graphics® and Cadence® tools with a set of scripts and macros
- ◆ Extensive VHDL/Verilog 2001 test bench
- ◆ Documentation:
  - ▶ Design Specification
  - ▶ Verification Specification
  - ▶ Test Plan
  - ▶ Integration Manual
- ◆ 30 days of technical support
- ◆ 90 days of warranty against defects

## DELIVERY OPTIONS

- ◆ EDIF netlist for FPGA and low volume production
- ◆ One-year maintenance
- ◆ On-site support and training



For more information on our IP portfolio visit [www.evatronix-ip.com](http://www.evatronix-ip.com)



## ELECTRONIC DESIGN DEPARTMENT

Dubois 16, 44-100 Gliwice, Poland  
T: +48 32 231 11 71  
F: +48 32 231 30 27

[info@evatronix-ip.com](mailto:info@evatronix-ip.com)  
[www.evatronix-ip.com](http://www.evatronix-ip.com)