

# HDLC

High-level Data Link Control Protocol Controller

## MAJOR FEATURES

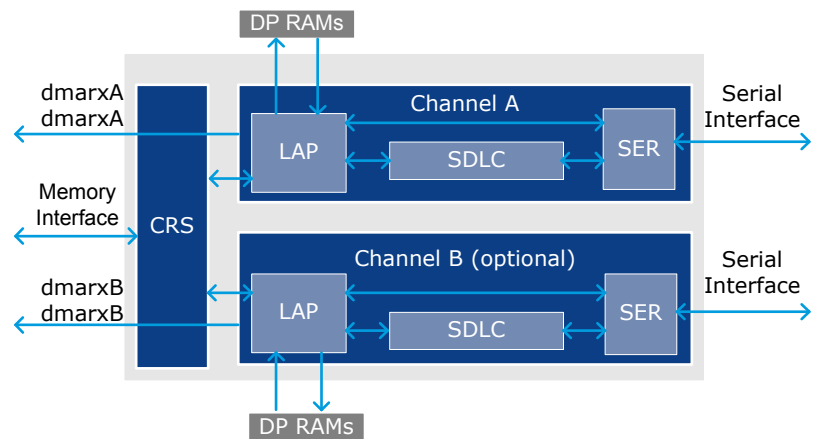
- ◆ HDLC protocol compatible
- ◆ Generic system bus interface
- ◆ LAPB/LAPD controlling machine
- ◆ Bit stuffing, flag generation and support for modem lines
- ◆ Receive Length Check
- ◆ Auto, non-auto and transparent modes of receive operation
- ◆ Interrupt or DMA transfer modes for receive transmit blocks
- ◆ 64-bytes long receive/transmit FIFOs
- ◆ Single or dual independent channel versions

## OVERVIEW

The **HDLC** controller IP implements High-Level Data Link Control (HDLC) protocol and its derivatives such as LAPB or LAPD. Link Access Procedure – Balanced (LAPB), the subset of HDLC protocol is used for the public networks that use the X.25 communications protocol. Link Access Procedure Channel D (LAPD) is intended for the ISDN implementations.

Functional features of the **HDLC** controller are based on Siemens® HSCX 82525 chip. Therefore programs written for HSCX chip can be used with the **HDLC** with minor changes.

## BLOCK DIAGRAM



# HDLC

## BENEFITS

- ◆ Hardware support for LAPB/LAPD means only minor frame processing in the target microcontroller
- ◆ Support for an external DMA controller speeds up data exchange between CPU and the **HDLC** controller
- ◆ Built-in timer for retransmission
- ◆ Support for line speeds of up to 10Mbit/s
- ◆ Shared interrupt line for 11 internal interrupts means no need for complicated interrupt controllers in CPU
- ◆ Very easy channel adding

## APPLICATIONS

- ◆ X.25 link control
- ◆ ISDN applications
- ◆ Physical link maintenance and quality monitoring of wide area networks
- ◆ General purpose telecommunication applications

## RELATED PRODUCTS

**HDLC Connectivity Platform** – an application platform that integrates the **R8051XC2** microcontroller with the **HDLC** controller.

## STANDARD DELIVERABLES

- ◆ VHDL/Verilog source code
- ◆ Synthesis support for Synopsys® tools with a set of synthesis scripts
- ◆ Simulation support for Mentor Graphics® and Cadence® tools with a set of scripts and macros
- ◆ Extensive test bench
- ◆ Documentation:
  - ▶ Design Specification
  - ▶ Verification Specification
  - ▶ Test Plan
  - ▶ Integration Manual
  - ▶ User Guide
- ◆ 30 days of technical support
- ◆ 90 days of warranty against defects

## DELIVERY OPTIONS

- ◆ EDIF netlist for FPGA and low volume production
- ◆ One-year maintenance
- ◆ On-site support and training



For more information on our IP portfolio visit [www.evatronix-ip.com](http://www.evatronix-ip.com)



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