

DISPLAY-CTRL

Ultra High Resolution Display Controller

MAJOR FEATURES

- ◆ RGB24 (8:8:8) and RGB15 (5:5:5) input data formats
- ◆ AMBA® system bus interface with 64-bit data master and 32-bit data slave interfaces
- ◆ Supports all regular and wide-screen resolutions from QVGA (320x240 pixels) to WUXGA (1920x1200)
- ◆ Output interface for Video DAC
- ◆ Progressive scanning mode support
- ◆ Fully configurable monitor frequencies and aspect ratios
- ◆ Hardware support for display functions
- ◆ Dedicated unidirectional DMA controller with burst transaction support
- ◆ Configurable internal FIFO
- ◆ Internal, event stimulated, interrupt request generation with masking capability
- ◆ Integrated test mode – generates color bar without any AHB bus transactions
- ◆ Little-endian architecture supported
- ◆ Power Save Mode

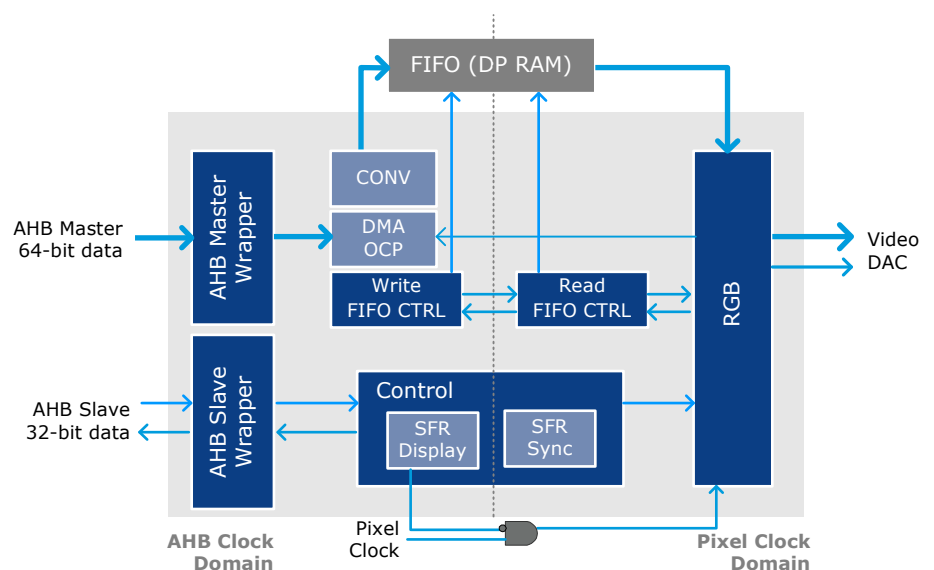
OVERVIEW

The **DISPLAY-CTRL** is a synthesizable IP intended for use with Video DACs with RGB interface up to 24 bits per pixel, Horizontal and Vertical synchronization signals, and Blanking (Data Enable) signal.

The controller accepts two different input color formats: RGB 24 bits per pixel and RGB 15 bits per pixel. All horizontal and vertical timing parameters such as horizontal/vertical front porch, back porch and sync intervals are programmable.

In order to facilitate the use of the **DISPLAY-CTRL** core in AMBA® bus-based microprocessor systems, an AMBA® AHB 64-bit Master and 32-bit Slave interfaces and FIFO controller are provided.

BLOCK DIAGRAM



DISPLAY-CTRL

BENEFITS

- ◆ Full HD and higher resolutions
- ◆ Seamless AMBA® AHB bus integration
- ◆ Variety of user-configurable options

APPLICATIONS

- ◆ Easy connection to DVI and HDMI interfaces, TFT controllers and analog RGB interfaces with a Video DAC compatible with RS-343A/RS-170 standards
- ◆ Portable video systems
- ◆ Advanced mobile phones with video capabilities

CONFIGURABILITY

- ◆ Depth of the FIFO memory
- ◆ The almost full level of FIFO
- ◆ The almost empty level of FIFO

STANDARD DELIVERABLES

- ◆ Verilog RTL source code
- ◆ Synthesis support for Synopsys® tools with a set of synthesis scripts
- ◆ Simulation support for Mentor Graphics® and Cadence® tools with a set of scripts and macros
- ◆ Extensive Verilog 2001 Testbench
- ◆ Documentation:
 - ▶ Design Specification
 - ▶ Verification Specification
 - ▶ Test Plan
 - ▶ Integration Manual
- ◆ 30 days of technical support
- ◆ 90 days of warranty against defects

DELIVERY OPTIONS

- ◆ EDIF netlist for FPGA and low volume production
- ◆ One-year maintenance
- ◆ On-site support and training



For more information on our IP portfolio visit www.evatronix-ip.com



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