

MAJOR FEATURES

- ◆ IEEE 802.3-2002 Standard compliance
- ◆ Configurable and monitorable through the Management Interface
- ◆ 1000BASE-X Auto-Negotiation process support for information data exchange with a link partner
- ◆ 8B-10B Data Encoder/Decoder
- ◆ Synchronization Module
- ◆ MAC frames encapsulation/de-encapsulation
- ◆ Data transmitting/receiving
- ◆ Carrier-extension transmitting/receiving
- ◆ Idle ordered sets for transmitting/receiving
- ◆ Standard Register Set
- ◆ PHY loopback mode support with MGM write control register command

MAC-1G PCS

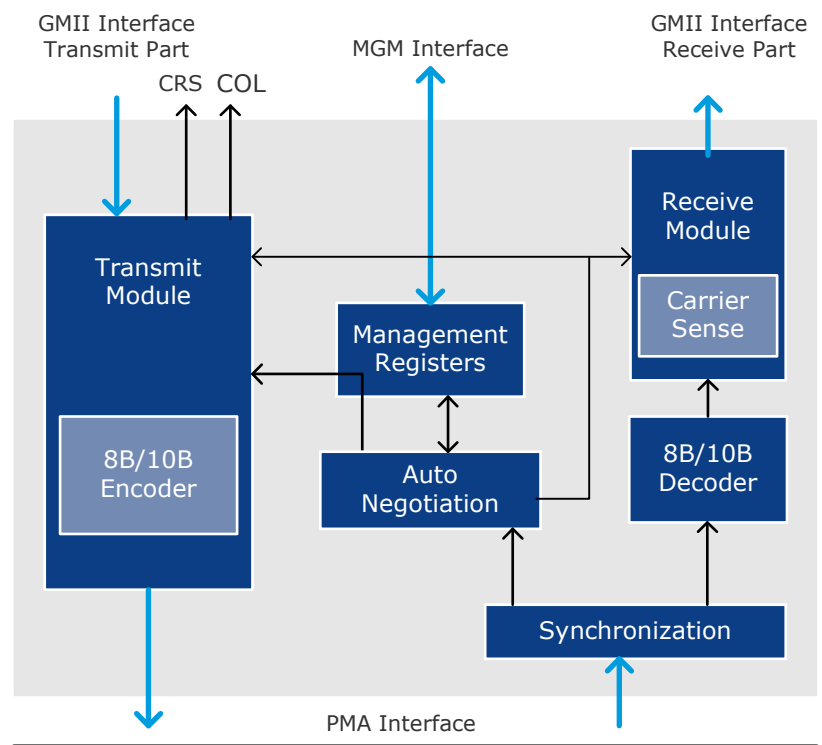
Gigabit Ethernet MAC Controller Physical Coding Sublayer

OVERVIEW

The **MAC-1G PCS** is an IP core of a 1 Gigabit Physical Coding Sublayer (PCS) that meets all IEEE 802.3-2002 Standard requirements.

The **MAC-1G PCS** provides both PCS interfaces - GMII and PMA. It also features the Management Interface (MGM) for communication with the Station Management (STA).

BLOCK DIAGRAM



MAC-1G PCS

BENEFITS

- ◆ Ethernet 100BASE-X support
- ◆ Possibility for FPGA implementation with 8B-10B Data Encoder/Decoder located in built-in memory blocks
- ◆ Perfect for integrating an Ethernet MAC controller with an optical transceiver through Physical Medium Attachment (PMA) sublayer

CONFIGURABILITY

The following parameters allow adjusting the **MAC-1G PCS** core to requirements of target application or technology:

- ◆ Auto-Negotiation
- ◆ Base page configuration

APPLICATIONS

- ◆ Ethernet 100BASE-X
- ◆ Repeaters and normal non-repeater devices

RELATED PRODUCTS

MAC-1G –the most feature-rich controller in the Evatronix MAC family. It operates at 10/100/1000 Mbps speed modes and contains the integrated descriptor based DMA. Its features include MII PHY management, Flow Control, and a full set of Statistical Counters.

STANDARD DELIVERABLES

- ◆ VHDL or Verilog source code
- ◆ Synthesis support for Synopsys® tools with a set of synthesis scripts
- ◆ Simulation support for Mentor Graphics® or Cadence® tools with a set of scripts and macros
- ◆ Extensive test bench
- ◆ Additional documentation:
 - ▶ Design Specification
 - ▶ Verification Specification
 - ▶ Test Plan
 - ▶ Integration Manual
- ◆ 30 days of technical support
- ◆ 90 days of warranty against defects

DELIVERY OPTIONS

- ◆ EDIF netlist for FPGA and low volume production
- ◆ Evaluation system
- ◆ One-year maintenance
- ◆ On-site support



For more information on our IP portfolio visit www.evatronix-ip.com



ELECTRONIC DESIGN DEPARTMENT

Dubois 16, 44-100 Gliwice, Poland
T: +48 32 231 11 71
F: +48 32 231 30 27

info@evatronix-ip.com
www.evatronix-ip.com