

DISPLAY-CTRL-4K

4K Digital Cinema Display Controller

MAJOR FEATURES

- ◆ Maximum supported screen size of 8190x8191 pixels
- ◆ Maximum supported resolutions depend on target technology
- ◆ Example resolutions supported in 40nm LP process:
4096x4096p 24fps 36-bit/pixel,
4096x2160p 30fps 36-bit/pixel,
1920x1200p 60fps 48-bit/pixel
- ◆ Choice of video output interface between RGB pixel data, HSYNC/ VSYNC and Data Enable (BLANK) signals
- ◆ Progressive scanning mode support
- ◆ Fully configurable screen resolutions and aspect ratios
- ◆ Configurable polarization of HSYNC and VSYNC signals
- ◆ AXI master interface to the system memory
- ◆ AXI slave interface to the host controller
- ◆ Configurable internal FIFO
- ◆ Internal, event stimulated, interrupt request generation with masking capability
- ◆ Integrated test mode – generates color bar without any AXI bus transactions
- ◆ Power Save Mode

OVERVIEW

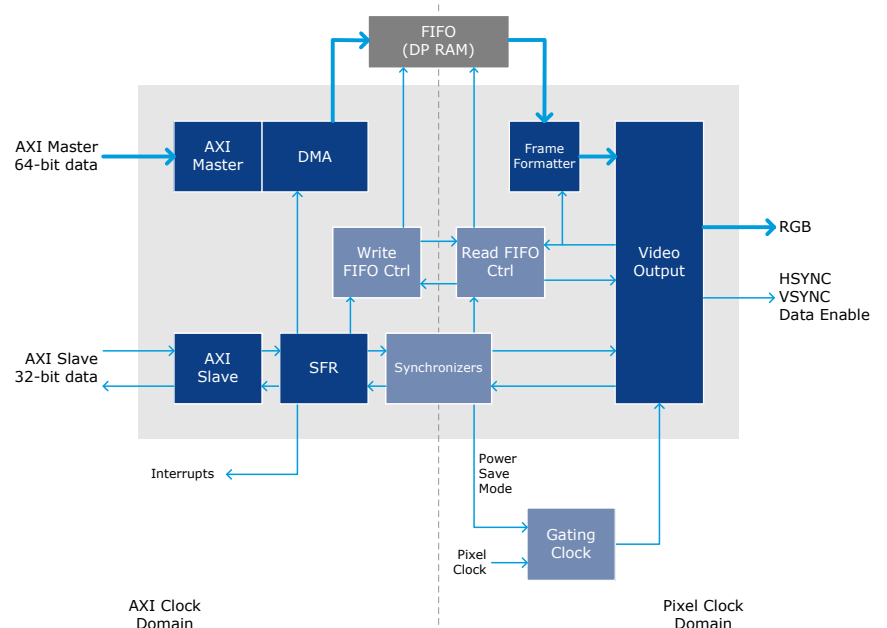
The **DISPLAY-CTRL-4K** is a synthesizable core intended for use in the AMBA® AXI bus-based microprocessor systems. It is a complete module of a digital video data path, which is transferred directly to the image display device interfaces such as DVI, HDMI or DisplayPort transmitters.

The display controller supports a wide range of resolutions in both standard and widescreen formats. The maximum screen size is 8190 by 8191 pixels, and the actual supported resolution depends on target technology.

The standard video data output is the most popular 24-bit per pixel RGB format. However, others formats like 30-bit, 36-bit, 48-bit per pixel or other can be easily implemented according to user requirements.

The data format in which the controller takes information from the system memory and stores in the FIFO is typical two 24-bit pixels per 64-bit data, but other data formats are also supported.

BLOCK DIAGRAM



DISPLAY-CTRL-4K

BENEFITS

- ◆ Configurable screen resolutions according to VESA or CEA standards or specific user requirements.
- ◆ All horizontal and vertical timing parameters are programmable via Special Function Registers (SFR)
- ◆ Seamless AMBA® AXI bus integration, with support for multiple outstanding transactions and long bursts support
- ◆ Glue-less connection to any AXI memory controller
- ◆ Independent from external memory type, and tolerant to external memory access latency

CONFIGURABILITY

- ◆ Width of the AXI Master read data bus
- ◆ Width of the AXI Master address bus
- ◆ Width of AXI Slave address bus
- ◆ ID Tag value for arid0m signal generated by the AXI Master
- ◆ Depth of the FIFO memory

APPLICATIONS

- ◆ Easy connection to DVI, HDMI and DisplayPort transmitters, TFT controllers and standard RGB interfaces with a Video DAC compatible to RS-343A/RS-170 standards
- ◆ Portable video systems
- ◆ Advanced mobile phones with video capabilities

STANDARD DELIVERABLES

- ◆ Verilog RTL source code
- ◆ Synthesis support for Synopsys® tools with a set of synthesis scripts
- ◆ Simulation support for Mentor Graphics® and Cadence® tools with a set of scripts and macros
- ◆ Extensive Verilog 2001 Testbench
- ◆ Documentation:
 - ▶ Design Specification
 - ▶ Verification Specification
 - ▶ Test Plan
 - ▶ Integration Manual
- ◆ 30 days of technical support
- ◆ 90 days of warranty against defects

DELIVERY OPTIONS

- ◆ EDIF netlist for FPGA and low volume production
- ◆ VHDL source code
- ◆ One-year maintenance
- ◆ On-site support and training



For more information on our IP portfolio visit www.evatronix-ip.com



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