

# C6502

MOS Technology® 6502-compatible Microprocessor

## MAJOR FEATURES

- ◆ MOS Technology® 6502 compliant
- ◆ Control Unit with both maskable and non-maskable interrupts
- ◆ 8-bit Instruction Decoder with 56 instructions and 151 opcodes
- ◆ 8-bit ALU for decimal and binary arithmetic as well as logical/ logical shift operations
- ◆ External Memory interface addressing up to 64KB of memory by 13 addressing modes

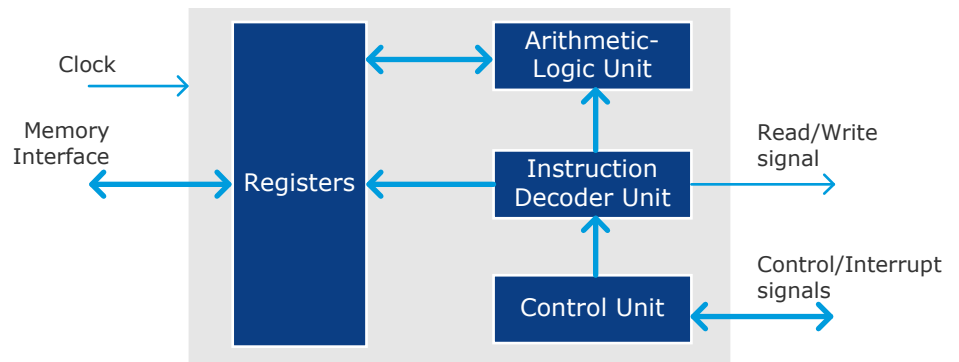
## OVERVIEW

The **C6502** is a fast 8-bit microprocessor IP that implements the same instruction set as the MOS Technology® 6502. The **C6502** provides software and hardware interrupts for interfacing external devices.

With thirteen addressing modes, including indirect index and zero page, the **C6502** is able to address up to 64KB of external memory with two byte long instructions.

The 8-bit arithmetic-logic unit can operate on signed and unsigned binary numbers as well as binary-coded decimal numbers.

## BLOCK DIAGRAM



# C6502

## BENEFITS

- ◆ 6502 architecture popularity results in a large variety of industry-certified software ready to be used with the core
- ◆ Obsolete IP cores, on contrary to original chips, can be easily integrated in more advanced SoC designs targeted to FPGAs or ASICs
- ◆ Having the IP core of the processor guarantees independence from the chip vendor
- ◆ Possibility to modify the instruction list according to customer's application

## APPLICATIONS

- ◆ 8-bit data processing applications
- ◆ Low power consumption applications
- ◆ High speed control systems
- ◆ Microcomputer systems

## PRODUCT VERSIONS

**C6510** – a **C6502** microprocessor equipped with a parallel bidirectional port. Widely used in the Commodore C64.

**C6502C** – a **C6502** microprocessor equipped with a HALT signal to control tri-state output buffers. Widely used in the Atari 130XE.

## STANDARD DELIVERABLES

- ◆ VHDL/Verilog source code
- ◆ Synthesis support for Synopsys® tools with a set of synthesis scripts
- ◆ Simulation support for Mentor Graphics® and Cadence® tools with a set of scripts and macros
- ◆ Extensive VHDL/Verilog 2001 test bench
- ◆ Documentation:
  - ▶ Design Specification
  - ▶ Verification Specification
  - ▶ Test Plan
  - ▶ Integration Manual
  - ▶ User Guide
- ◆ A collection of 6502 assembler programs which are executed directly by the test bench
- ◆ 30 days of technical support
- ◆ 90 days of warranty against defects

## DELIVERY OPTIONS

- ◆ EDIF netlist for FPGA and low volume production
- ◆ Evaluation system for proprietary **EB5-Tiny** board
- ◆ One-year maintenance
- ◆ On-site support and training



For more information on our IP portfolio visit [www.evatronix-ip.com](http://www.evatronix-ip.com)



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